

DUAL DIE MEMORY

ABSTRACT OF THE DISCLOSURE

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A double-sized chip assembly and method is provided for two back-to-back integrated-circuit chips which both have the same fabrication mask sets. An electrically-selectable bonding-pad connection option alternatively provides a standard, non-reversed, option NRO for a bonding-pad layout and
10 a non-standard, reversed option RO for the layout of the bonding-pads. The double-sized, back-to-back, wire-bonded integrated-circuit chip assembly and method includes a pair of integrated-circuit chips, each having one or more reversible wire-bonding-pads. One of the chips has its wire-bonding-pads electrically reversed such that the wire-bonding pads on both chips are
15 located near each other to accommodate wire-bonding to a common bonding finger of a lead frame. A bonding-option wire-bonding-pad has an external voltage applied to it to indicate whether the integrated-circuit chip is to provide a standard pattern for the reversible wire-bonding-pads, or a reversed pattern for the reversible wire-bonding-pads. A voltage sensor
20 circuit senses the voltage applied to the bonding-option wire-bonding-pad and alternatively generates either a standard NRO gate control signal or a non-standard, reversed RO gate control signal from the voltage state of the bonding-option wire-bonding-pad.